MULTILAYER PASSIVE COMPONENTS FOR UNIPLANAR Si/SiGe MMICs

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ABSTRACT

This paper describes results for novel multilayer passive components, fabricated on silicon substrates for Si/SiGe uniplanar MMICs. Results are compared for high resistivity silicon, high resistivity silicon with an added polyimide layer, and silicon with silicon dioxide (to represent SOI bonded silicon technology). The components that have been characterized include CPW and TFMS transmission lines and couplers, inductors, capacitors, and planar transformers.

INTRODUCTION

Both silicon bipolar transistors (BJTs) and SiGe HBTs have recently demonstrated excellent microwave and even mm-wave performance potential. Already, very significant results have been achieved for silicon and SiGe MMICs [1,2]. In order to obtain full performance from the active devices, it is important that passive components with low loss and low parasitic capacitance are made available. Mostly, high resistivity silicon has been used to make this possible, but this has the disadvantage of requiring expensive high purity substrates. Other techniques, such as SOI technology have been used but relatively little experimental data has been published on the performance of microwave passive components such as transmission lines and couplers. In this paper, the use of multilayer techniques for the realization of low loss Si/SiGe MMIC passive components is described. Multilayer techniques have been extensively researched for GaAs MMICs, with the aim of achieving high packing density [3-4]. For GaAs MMICs it is usually the case that multilayer passive components are significantly more lossy than the standard equivalents. However, for silicon substrates, where the substrate is not semi-insulating, it is likely that multilayer components can offer both smaller size and lower loss and parasitic capacitance than standard components placed directly on the substrate.

FABRICATION

All the components were fabricated at King's College using an experimental circuit fabrication process which provides three aluminum metal layers with polyimide spacer dielectric layers. Aluminum and polyimide are widely used for silicon circuits in the microelectronics industry. The chosen polyimide was Hitachi PIQ-13 which has nominal bulk values of er=3.4 and tand=0.001. The polyimide was spin-coated at 3000rpm for 40 seconds, yielding a cured film thickness of 2um (nominally; the actual thickness at any point may vary according to the local features because of the planarisation effect). The plasma etching of polyimide windows and the creation of novel 3-D structures was extensively investigated in the earlier work on GaAs substrates [5].

In this paper three substrate configurations have been compared:
(1) High resistivity silicon (rho=8350ohm-cm)
(2) High resistivity silicon with a polyimide superstrate (Fig. 1(a)).
(3) Silicon with a silicon dioxide layer (Fig. 1(b)).

Type (2) is intended to increase the performance of the passive components whilst avoiding complex extra process steps. Type (3) is intended to mimic the passive components of silicon-on-insulator (SOI, or bonded silicon) technology, which is an important means of realising high performance devices with reduced parasitic capacitance (especially collector - substrate capacitance). Here, the dioxide layer is 5000Å thick and the substrate resistivity is 40 ohm-cm.

DESIGN AND CHARACTERIZATION OF MULTILAYER PASSIVE COMPONENTS

Fig. 2 shows a photograph of the test wafer, with approximately 50 test components. Here, a selection of measured results is presented to demonstrate that performance comparable to GaAs can be achieved.

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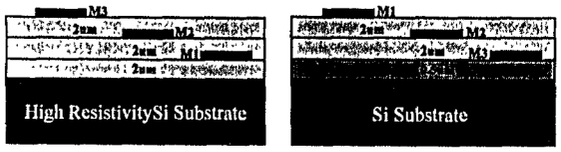


(a) (b)

Fig. 1. Multilayer structure, a) Three polyimide and three metal layers, b) One SiO_2 and two polyimide layers.

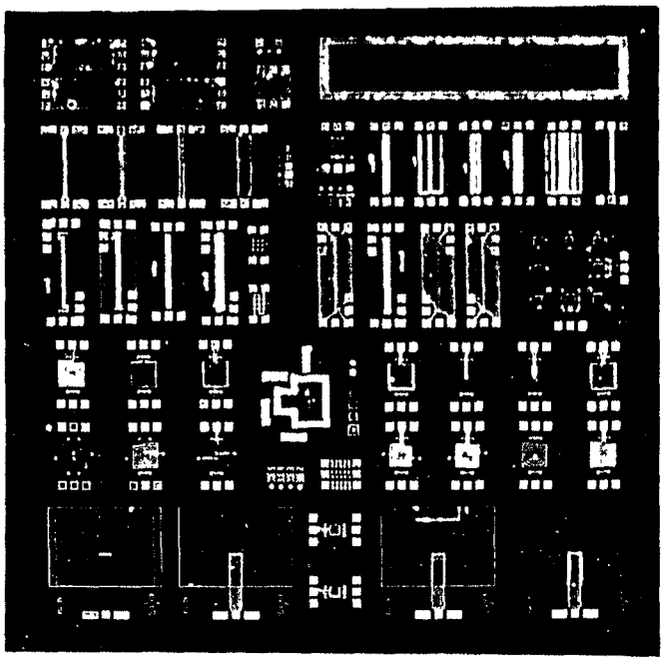


Fig. 2. Photograph of the test wafer.

(a) Lumped elements: Inductors, planar transformers and capacitors

Fig. 3 shows a photograph of two typical CPW lumped elements; a capacitor and a 5 turn single layer inductor. The capacitor shown uses three metal plates; the M1 and M3 plates are connected together at the edge, yielding double the capacitance for a given area. Fig. 4 (a) shows the equivalent circuit for such a capacitor with dimensions of 400 x 400 um, yielding a prime capacitance of 5pF, for substrate type (2). Fig. 4 (b) shows the equivalent circuit of the 5 turn inductor on substrate type (2) with the spiral track on metal layer M3; compared with an equivalent GaAs inductor the only significant degradation is the introduction of the 900 ohm parasitic resistances to ground. Fig. 5 shows a comparison of the measured and modelled S21 and S11 of the CPW inductor, indicating good agreement up to 20 GHz, and a self-resonant frequency of 15 GHz.

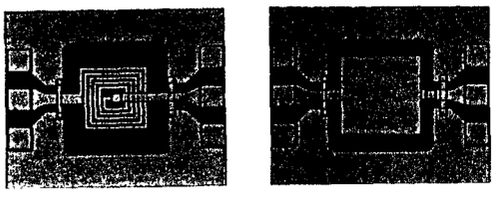


Fig.3. Photograph of two CPW elements.

The purpose of using multilayer inductors is to achieve high inductance-per-unit-area and/or higher Q-factor. Low loss is achieved by using a plated-up coil (all metal layers used simultaneously and connected throughout their length with vias), and/or by mounting the coil on top of added dielectric layers away from the silicon. The latter is particularly important if low cost wafers are preferred. High inductance-per-unit-area is achieved with the stacked spiral technique, in which two or more spirals are interwound to form a single inductor; the mutual inductance between spirals provides a very significant increase in total inductance. Fig. 4 (c) shows the equivalent circuit of a 5 turn two-layer stacked spiral inductor on substrate type (2); the model shows that a greatly increased inductance is achieved (20 nH), although the self-resonant frequency is reduced significantly (to < 5 GHz).

Planar spiral transformers [6,7] achieved acclaim through the pioneering work at Honeywell and Pacific Monolithics. The attraction is that a spiral transformer can provide DC bias injection, DC blocking and matching in a small area. Recent work at King's [8] showed that multilayer transformers on GaAs could offer improved performance when applied to transformer-coupled FET amplifiers. Here, the same transformers have been tested on silicon substrates and the performance is almost the same. Fig. 6 shows a simulation of a single-stage transformer-coupled amplifier using a "typical" BJT (ft=20 GHz) and indicates the performance that could be expected from a complete uniplanar Si MMIC amplifier.

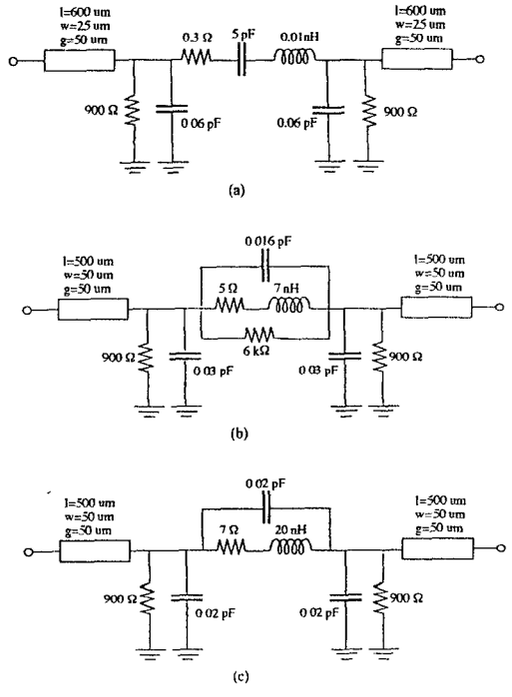


Fig.4. Equivalent circuits for, a) Capacitor, b) 5 turn inductor, c) 5 turn stacked spiral inductor.

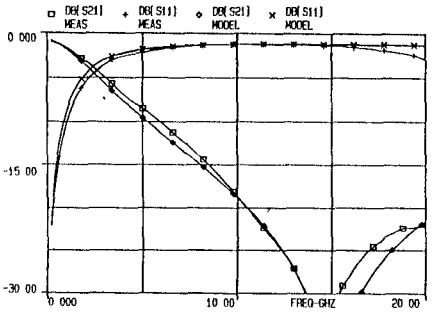


Fig. 5. Comparison of measured and modelled results for 5 turn inductor.

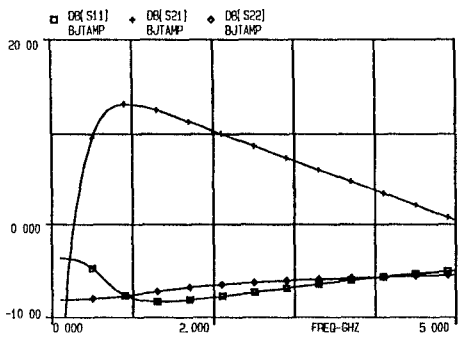


Fig. 6. Simulation of basic transformer-coupled BJT amplifier.

(b) CPW Transmission lines and couplers

Multilayer techniques allow the realization of miniature 3 dB couplers since overlaid structures can readily be used instead of interdigitated structures. Investigation of GaAs multilayer couplers has shown that excellent performance is obtainable [9]. Fig. 7 shows a photograph of the CPW overlaid coupler on silicon. The measured response when fabricated on the silicon/polyimide and silicon/silicon dioxide are presented in Fig. 8 (a) and (b) [Ref. 10 describes the GaAs versions]. On high resistivity silicon the loss is 1 dB at 26 GHz and the coupler is suited for many applications: On the SOI substrate the loss is 2dB at 26 GHz, so the coupler is too lossy for power combining but remains useful for mixers and similar applications requiring equal power split with 90 degree phase difference.

Characterizing the loss of MMIC transmission lines can be difficult because when measuring quite short lengths of line the measurement uncertainties mask any genuine but small differences between the loss on the different substrate configurations. Here, a CPW dual-mode ring resonator [11] has been tested successfully, using a combination of CPW lines and MIM capacitors, and enables a close comparison of relative loss performance to be made. The photograph is shown in Fig. 9, and the measured response on various substrates is compared in Fig. 10. This confirms the expected results: GaAs yields the lowest loss, followed by types (2), (1) and (3) in that order. With the additional polyimide layer the high resistivity silicon substrate gives performance almost equal to the GaAs ring.

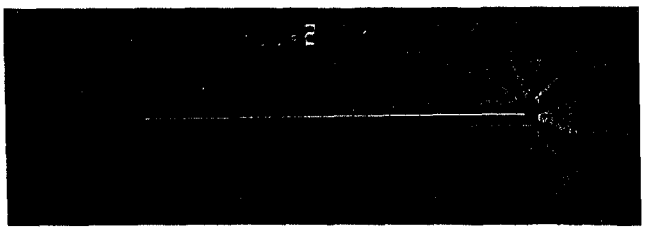
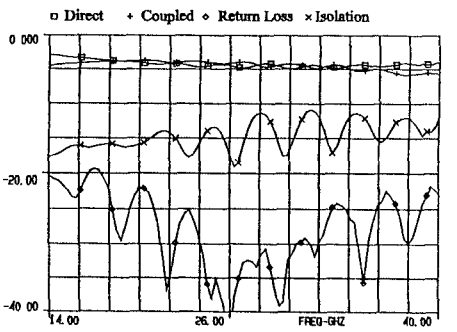
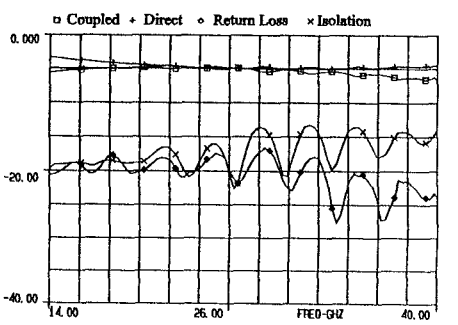


Fig. 7 Photograph of the multilayer coupler.



(a)



(b)

Fig. 8. Measured coupler response, a) Three polyimide layers, b) One SiO_2 and two polyimide layers.

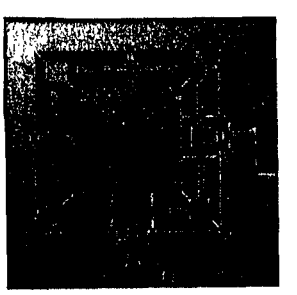


Fig. 9. Photograph of the ring resonator.

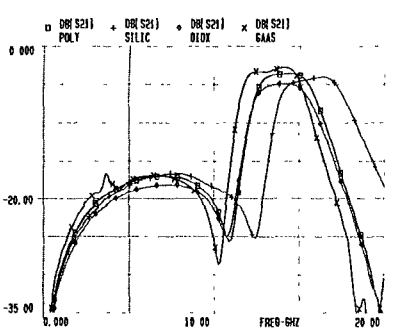


Fig. 10. Measured ring resonator results.

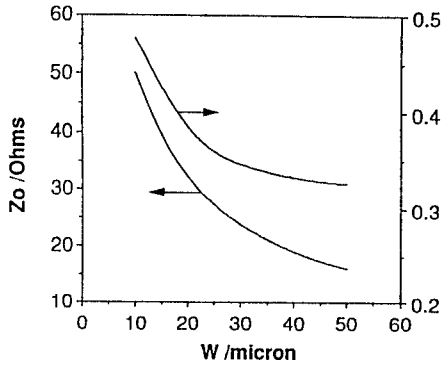


Fig. 11. Characteristic impedance and loss vs. strip width.

(c) Thin-film microstrip lines

Thin-film microstrip [12] is ideal for silicon MMICs because the signal is contained within the thin dielectric, and the silicon need not have high resistivity. A set of TFMS lines has been characterized with widths in the range 10 to 50 microns, with the signal conductor on layer M3 and the ground plane on layer M1. Each line was measured and an equivalent circuit fitted with Touchstone™. Fig. 11 summarizes the results by plotting the characteristic impedance and loss vs. conductor strip width. An impedance range of 15 to 50 ohms has been achieved with the 3 layer process. There is a trade-off between size and performance; adding extra polyimide layers enables a lower loss but wider TFMS line to be fabricated. Also, note that there is a seldom-mentioned drawback with these TFMS lines; the εr of polyimide and other common dielectrics is lower than that of GaAs or silicon. As a result the TFMS lines are longer than the standard microstrip lines. It is expected that alternative materials will be used in the future to overcome this drawback.

CONCLUSIONS

This work has illustrated that multilayer techniques can produce important performance benefits for passive elements in silicon MMIC applications. This is an interesting contrast to the GaAs experience where multilayer techniques have not been widely adopted because of the high loss associated with them. Here a wide range of CPW passive components has been presented, with performance almost identical to previous reported results for a GaAs substrate. The experimental Si MMIC fabrication process uses completely standard materials and techniques and is compatible with BJTs and Si-Ge HBTs, both of which have already been integrated with CMOS VLSI circuitry. This potential combination of good microwave passive components, high ft transistors, and digital signal processing capabilities is extremely attractive for communications transceivers in the future.

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